

APPLICATION FOR UNITED STATES PATENT

in the name of

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for

**MARKING UNRELIABLE SYMBOLS IN A HARD DISK
DRIVE READ BACK SIGNAL**

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MARKING UNRELIABLE SYMBOLS IN A HARD DISK DRIVE READ BACK SIGNAL

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Patent Application Serial No. 60/445,291 entitled "A Method for Marking Unreliable Symbols in the Hard Disk Drive Read Back Signal," filed February 4, 2003, the disclosure thereof incorporated by reference herein in its entirety.

BACKGROUND

[0002] The present invention relates to detection of signals on communications channels. More particularly, the present invention relates to marking unreliable symbols read back from a hard disk drive.

[0003] Data stored on magnetic media, such as hard disk drives, are typically encoded using an error-correction code, such as a Reed-Solomon code, so that errors that occur during storage and read back of the data can be detected and corrected. In conventional systems, the read back signal is typically detected by a channel detector, such as a Viterbi detector, that generates multi-bit symbols based on the read back signal. These symbols often include errors due to imperfect detection and noise.

[0004] Conventional systems typically include an error-correction decoder, such as a Reed-Solomon decoder, that uses the error-correction code in the data to correct these errors. Each error-correction code, and its associated decoder, has a power t , and can correct t symbol errors in the read back data sequence. When a sequence has more than t symbol errors, the decoder cannot correct the symbol, and typically triggers a retry, in which the data is read back from the disk a second time, detected again, and decoded again. This process can repeat until the detected sequence has t or fewer symbol errors, in which case it can be corrected by the decoder. Of course, this repetitive retry process consumes significant amounts of time, thus reducing the rate at which data can be read back from the hard disk drive.

SUMMARY

[0005] In general, in one aspect, the invention features a hard disk drive system comprising a hard disk drive comprising a channel; a channel detector adapted to receive a first signal representing a channel sequence from the channel, and to produce a first detected sequence based on the first signal, wherein the first detected sequence comprises a plurality of symbols; a decoder comprising an error-correction decoder adapted to produce first data based on the first detected sequence when a number of symbols in error in the first detected sequence is less than, or equal to, a predetermined number, and to assert a failure indication when the number of symbols in error in the first detected sequence is greater than the predetermined number; and a controller adapted, when the error-correction decoder asserts the failure indication for the first detected sequence, to cause the channel detector to receive a second signal representing the channel sequence from the channel, and to produce a second detected sequence based on the second signal, wherein the second detected sequence comprises a plurality of symbols, and identify corresponding symbols of the first and second detected sequences that differ; wherein the decoder produces second data based on the symbols identified by the controller and at least one of the first and second detected sequences.

[0006] Particular implementations can include one or more of the following features. The error-correction decoder is further adapted to produce the second data based on the symbols identified by the controller and at least one of the first and second detected sequences. The controller is further adapted to generate a candidate sequence based on the first and second detected sequences; and the error-correction decoder is further adapted to produce the second data based on the candidate sequence. The controller is further adapted to generate the candidate sequence by replacing k of the identified symbols of one of the first and second detected sequences with k respective corresponding symbols of the other of the first and second detected sequences, wherein k is greater than, or equal to, one. The error-correction decoder is a Reed-Solomon decoder. The channel is selected from the group comprising a magnetic recording channel; and an optical recording channel. Implementations comprise an interface circuit adapted to output the second data.

[0007] In general, in one aspect, the invention features an apparatus comprising a channel detector adapted to receive a first signal representing a channel sequence from a channel, and to produce a first detected sequence based on the first signal,

wherein the first detected sequence comprises a plurality of symbols; and a decoder comprising an error-correction decoder adapted to produce first data based on the first detected sequence when a number of symbols in error in the first detected sequence is less than, or equal to, a predetermined number, and to assert a failure indication when the number of symbols in error in the first detected sequence is greater than the predetermined number; and a controller adapted, when the error-correction decoder asserts the failure indication for the first detected sequence, to cause the channel detector to receive a second signal representing the channel sequence from the channel, and to produce a second detected sequence based on the second signal, wherein the second detected sequence comprises a plurality of symbols, and identify corresponding symbols of the first and second detected sequences that differ; wherein the decoder produces second data based on the symbols identified by the controller and at least one of the first and second detected sequences.

[0008] Particular implementations can include one or more of the following features. The error-correction decoder is further adapted to produce the second data based on the symbols identified by the controller and at least one of the first and second detected sequences. The controller is further adapted to generate a candidate sequence based on the first and second detected sequences; and the error-correction decoder is further adapted to produce the second data based on the candidate sequence. The controller is further adapted to generate the candidate sequence by replacing k of the identified symbols of one of the first and second detected sequences with k respective corresponding symbols of the other of the first and second detected sequences, wherein k is greater than, or equal to, one. The error-correction decoder is a Reed-Solomon decoder. The channel is selected from the group comprising a magnetic recording channel; an optical recording channel; a wired communications channel; a wireless communications channel; and an optical communications channel. Implementations comprise an integrated circuit comprising the apparatus of claim 13.

[0009] In general, in one aspect, the invention features a method and computer program comprising receiving a first signal representing a channel sequence from a channel; producing a first detected sequence based on the first signal, wherein the first detected sequence comprises a plurality of symbols; producing first data based on the first detected sequence when a number of symbols in error in the first detected sequence is less than, or equal to, a predetermined number; asserting a failure indication when the number of symbols in error in the first detected sequence is greater than the predetermined number; when the failure indication is asserted for the

first detected sequence, receiving a second signal representing the channel sequence from the channel, producing a second detected sequence based on the second signal, wherein the second detected sequence comprises a plurality of symbols, and identifying corresponding symbols of the first and second detected sequences that differ; and producing second data based on the identified symbols and at least one of the first and second detected sequences.

[0010] Particular implementations can include one or more of the following features. Producing the second data comprises generating a candidate sequence based on the first and second detected sequences; and producing the second data based on the candidate sequence. Generating the candidate sequence comprises replacing k of the identified symbols of one of the first and second detected sequences with k respective corresponding symbols of the other of the first and second detected sequences, wherein k is greater than, or equal to, one. The channel sequence is encoded using a Reed-Solomon code. The channel is selected from the group comprising a magnetic recording channel; an optical recording channel; a wired communications channel; a wireless communications channel; and an optical communications channel.

[0011] The details of one or more implementations are set forth in the accompanying drawings and the description below. Other features will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

[0012] FIG. 1 shows a hard disk drive system that includes a read channel device for processing a read back signal from a hard disk.

[0013] FIG. 2 shows a signal detector that can serve as the signal detector of FIG. 1 according to a preferred embodiment.

[0014] FIG. 3 shows a process that can be executed by the signal detector of FIG. 2 according to a preferred embodiment.

[0015] FIG. 4 compares a detected sequence having eight symbols with the correct sequence.

[0016] FIG. 5 shows a process that can be executed by the decoder of FIG. 2 according to a preferred embodiment.

[0017] The leading digit(s) of each reference numeral used in this specification indicates the number of the drawing in which the reference numeral first appears.

DETAILED DESCRIPTION

[0018] While embodiments of the present invention are described with respect to a communication channel in a magnetic hard disk, in other embodiments, the communication channel is in a different type of recording media channel, such as an optical disk, magnetic tape, and so on, a wired, wireless or optical recording channel, and the like.

[0019] FIG. 1 shows a hard disk drive system 100 that includes a read channel device 102 for processing a read back signal from a hard disk 104. Read channel device 102 can include an optional signal receiver 106 to receive and condition the read back signal. A signal detector 108 detects and decodes the conditioned read back signal to generate data. An optional interface circuit 110 outputs the data, for example to an input/output bus in a computer system.

[0020] FIG. 2 shows a signal detector 200 that can serve as signal detector 108 of FIG. 1 according to a preferred embodiment. Signal detector 200 includes a channel detector 202 and a decoder 204 that includes an error-correction decoder 206 and a controller 208. Channel detector 202 preferably comprises a Viterbi detector, but can instead comprise some other sort of channel detector. Error-correction decoder 206 preferably comprises a Reed-Solomon decoder, but can instead comprise some other sort of error-correction decoder.

[0021] FIG. 3 shows a process 300 that can be executed by signal detector 200 of FIG. 2 according to a preferred embodiment. Channel detector 202 receives a signal s1 representing a channel sequence from a channel (step 302). For example, referring to the hard disk drive system 100 of FIG. 1, read channel device 102 reads data from hard disk 104, and provides signal s1, preferably through optional signal receiver 106, to channel detector 202. Channel detector 202 produces a detected sequence d1 based on signal s1 (step 304), according to well-known techniques such as Viterbi detection.

[0022] Detected sequence d1 comprises a plurality of symbols, each comprising a plurality of bits. Each symbol may contain errors introduced by noise sources such as the channel, read channel device 102, and the like. FIG. 4 compares a detected sequence d1 having eight symbols with the correct sequence d. Referring to FIG. 4, it is clear that detected sequence d1 contains two errors. The second symbol of detected sequence d1 is 21 while the second symbol of correct sequence d is 22. And the eighth symbol of detected sequence d1 is 81 while the eighth symbol of correct

sequence d is 82. Therefore an error-correction decoder 206 with a power of one would be unable to correct detected sequence d1.

[0023] Error-correction decoder 206 produces data based on detected sequence d1 when the number of symbols in error in the detected sequence d1 is less than, or equal to, the power of error-correction decoder 206 (steps 306 and 308), and asserts a failure indication when the number of symbols in error in the detected sequence d1 is greater than the power of error-correction decoder 206.

[0024] When error-correction decoder 206 asserts the failure indication for detected sequence d1, controller 208 causes channel detector 202 to receive a second signal s2 representing the channel sequence from the channel (steps 306 and 310). For example, referring again to the hard disk drive system 100 of FIG. 1, read channel device 102 reads the data from hard disk 104 a second time, and provides signal s2, preferably through optional signal receiver 106, to channel detector 202. Channel detector 202 produces a detected sequence d2 based on signal s2 (step 312), preferably according to the same technique used to produce detected sequence d1.

[0025] Detected sequence d2 comprises a plurality of symbols, each comprising a plurality of bits. Each symbol in detected sequence d2 may contain errors introduced by noise sources such as the channel, read channel device 102, and the like. But because these noise sources vary with time, the symbols of detected sequences d1 and d2 will likely have different errors. Referring again to FIG. 4, it is clear that sequence d2 contains two errors. The fourth symbol of detected sequence d2 is 4 while the fourth symbol of correct sequence d is 41. And the seventh symbol of detected sequence d2 is 72 while the seventh symbol of correct sequence d is 71. Therefore an error-correction decoder 206 with a power of one would be unable to correct detected sequence d2.

[0026] Error-correction decoder 206 produces data based on detected sequence d2 when the number of symbols in error in the detected sequence d1 is less than, or equal to, the power of error-correction decoder 206 (steps 314 and 316), and asserts a failure indication when the number of symbols in error in detected sequence d2 is greater than the power of error-correction decoder 206.

[0027] When error-correction decoder 206 asserts the failure indication for detected sequence d2, controller 208 identifies corresponding symbols of detected sequences d1 and d2 that differ (step 318). For example, referring to FIG. 4, error-correction

decoder 206 identifies the second, fourth, seventh, and eighth symbols because these symbols have different values in detected sequences d1 and d2.

[0028] Decoder 204 produces data based on the symbols identified by controller 208 (in step 318) and at least one of detected sequences d1 and d2 (step 320). Of course, if controller 208 asserts the failure indication for this operation, steps 312 through 320 can be repeated to read the data from the channel a third time, produce a third detected sequence d3, and, if necessary, identify corresponding symbols of at least two of the detected sequences d1, d2, and d3 that differ, and produce data based on the identified symbols and at least one of detected sequences d1, d2, and d3. This process can be repeated as many times as necessary.

[0029] Some error-correction decoders, such as Reed-Solomon decoders, can improve their performance when symbols suspected of errors are identified to them. In one embodiment, controller 208 passes the identities of the corresponding symbols of detected sequences d1 and d2 that differ (obtained in step 318) to error-correction decoder 206. Error-correction decoder 206 then produces data based on the symbols identified by controller 208 and at least one of detected sequences d1 and d2 according to well-known erasure decoding techniques.

[0030] In another embodiment, decoder 204 produces data based on the symbols identified by controller 208 (in step 318) and at least one of detected sequences d1 and d2 according to process 500 shown in FIG. 5. Controller 208 generates a candidate sequence based on detected sequences d1 and d2 (step 502). Preferably controller 208 generates the candidate sequence by replacing one or more of the identified symbols (identified in step 318 of FIG. 3) of one of detected sequences d1 and d2 with the respective corresponding symbols of the other of detected sequences d1 and d2. For example, referring to FIG. 4, controller 208 generates a candidate sequence c1 by replacing the second symbol of detected sequence d1 (having a value of 21) with the second symbol of detected sequence d2 (having a value of 22).

[0031] Error-correction decoder 206 produces data based on candidate sequence c1 when the number of symbols in error in candidate sequence c1 is less than, or equal to, the power of error-correction decoder 206 (steps 504 and 506), and asserts a failure indication when the number of symbols in error in candidate sequence c1 is greater than the power of error-correction decoder 206.

[0032] When error-correction decoder 206 asserts the failure indication for candidate sequence c1, controller 208 generates a different candidate sequence (step 502) using

a different combination of the identified symbols (identified in step 318 of FIG. 3). For example, referring again to FIG. 4, controller 208 generates a different candidate sequence by replacing the eighth symbol of detected sequence d1 (having a value of 81) with the eighth symbol of detected sequence d2 (having a value of 82). This process is repeated until error-correction decoder 206 produces data based on the candidate sequence, or until all possible candidate sequences have been tried (step 508), in which case a decoding failure is declared (step 510).

[0033] The invention can be implemented in digital electronic circuitry, or in computer hardware, firmware, software, or in combinations of them. Apparatus of the invention can be implemented in a computer program product tangibly embodied in a machine-readable storage device for execution by a programmable processor; and method steps of the invention can be performed by a programmable processor executing a program of instructions to perform functions of the invention by operating on input data and generating output. The invention can be implemented advantageously in one or more computer programs that are executable on a programmable system including at least one programmable processor coupled to receive data and instructions from, and to transmit data and instructions to, a data storage system, at least one input device, and at least one output device. Each computer program can be implemented in a high-level procedural or object-oriented programming language, or in assembly or machine language if desired; and in any case, the language can be a compiled or interpreted language. Suitable processors include, by way of example, both general and special purpose microprocessors. Generally, a processor will receive instructions and data from a read-only memory and/or a random access memory. Generally, a computer will include one or more mass storage devices for storing data files; such devices include magnetic disks, such as internal hard disks and removable disks; magneto-optical disks; and optical disks. Storage devices suitable for tangibly embodying computer program instructions and data include all forms of non-volatile memory, including by way of example semiconductor memory devices, such as EPROM, EEPROM, and flash memory devices; magnetic disks such as internal hard disks and removable disks; magneto-optical disks; and CD-ROM disks. Any of the foregoing can be supplemented by, or incorporated in, ASICs (application-specific integrated circuits) .

[0034] A number of implementations of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Please list any additional

modifications or variations. Accordingly, other implementations are within the scope of the following claims.